FIG. 4*d* shows a wet etch using hydrofluoric acid of windows **410** and **420** in PSG layer **119**.

FIG. 4*e* shows deposition of aluminum film **430** (0.1–0.2 μm) as a high reflectivity layer.

FIG. 4*f* shows a wet etch (typically a mixture of phosphoric and nitric acid) Al to leave Al in mirror regions.

FIG. 4*g* shows etching of vias **133** to Si substrate **115** using CF_4/O_2 RIE with a photoresist mask.

FIG. 4*h* shows the deposited polysilicon layer of 1–2 μm thickness after being patterned to form hinge **155** for deflecting mirror **140**. Patterning of polysilicon hinges **155** is described in Wu, "Micromachining for Optical and Optoelectronic Systems", Proceedings of IEEE, vol. 85, p.1833, 1997 and Pister et al., "Microfabricated hinges", Sensors and Actuators, A: Physica v 33 n 3 p. 249–256, 1992 which are hereby incorporated by reference in their entirety. If the RIE etching step is done before deposition of the polysilicon layer, the polysilicon can be deposited in etched recess **135** to reduce surface roughness due to the etching.

FIG. 4*i* shows the etch of PSG layer **119** and SCS layer **130** to pattern deflecting mirror **140**, hinge **155** and access holes **137**. Holes **137** allow for the etchant used to release deflecting mirror **140** to reach insulating layer **116**. A typical size for holes **137** is 10 μm by 10 μm. Torsional mirror **150** is also defined in this step. Typical size for torsional mirror **150** in accordance with this invention is in the range of 1–2 mm square.

FIG. 4*j* shows the Ti—Au deposition of wettable metal bonding pads **111** and solder for solder bumps **110**. Solder is reflowed into solder bumps **110** by heating at temperatures<310° C. This leaves the finished, unreleased MEMS parts, along with precisely defined recess **135**, ready for the GaAs bonding step in FIG. 4.

FIG. 4*k* shows release of deflecting mirror **140** and hinge **155** by etching PSG layer **119** and insulator layer **116** by using a hydrofluoric (HF) based etch.

FIG. 4*l* shows placement of VCSEL **105** (thickness from 100–125 μm) into recess **135** for the GaAs bonding step. Solder bumps **110** can be defined on VCSEL **105** and VCSEL **105** is placed into recess **135** which approximately aligns the bumps to wettable metal bonding pads **111** and **113** due to the coordinated geometry of VCSEL **105**, recess **135**, wettable metal bonding pad **111** and solder bump **110** positions. Si Substrate **115** and VCSEL substrate **106** are heated to allow solder to flow and contact wettable metal bonding pads **113** on the bottom of VCSEL substrate **106**.

FIG. 4*m* shows hinges **155**, deflecting mirror **140**, torsional mirror **150** and VCSEL **105** bonded to glass substrate **101** or to SiN_x-coated or SiO_2-coated Si substrate **101**. Substrate **101** supports actuation electrodes **120** for torsional mirror **150**.

FIG. 4*n* shows raised deflecting mirror **140** locked with latch **168**. Angle of deflecting mirror **140** is fixed by the length of latch **168** and position of hole **165** at base of deflecting mirror **140**.

Linear arrays of lasers can be bonded in a similar way; the extent of the array being perpendicular to the cross section shown in FIGS. 3*a* and 3*b*.

While the invention has been described in conjunction with specific embodiments, it is evident to those skilled in the art that many alternatives, modifications, and variations will be apparent in light of the foregoing description. Accordingly, the invention is intended to embrace all other such alternatives, modifications, and variations that fall within the spirit and scope of the appended claims.

What is claimed is:

1. An integrated laser beam scanning structure comprising:

a wafer having a recess on a side;

a layer having a first region and a second region, said layer being attached to said side of said wafer having said recess;

a deflecting mirror fashioned from said first region of said layer;

a torsional mirror fashioned from said second region of said layer, said torsional mirror having a first side; and

a semiconductor light emitter mounted in said recess whereby a light beam emitted from said semiconductor light emitter is deflected by said deflecting mirror onto said first side of said torsional mirror.

2. The structure of claim **1** wherein said wafer is a silicon on oxide wafer.

3. The structure of claim **1** wherein said layer is a single crystal silicon layer.

4. The structure of claim **1** wherein said semiconductor light emitter is mounted in said recess using solder bumps.

5. The structure of claim **1** wherein said semiconductor light emitter is a VCSEL chip.

6. The structure of claim **1** wherein said recess is deep reactive ion etched.

7. The structure of claim **1** wherein said torsional mirror is actuated by a pair of electrodes.

8. The structure of claim **1** wherein a ferromagnetic thin film is attached to said first side of said torsional mirror.

9. The structure of claim **8** wherein said torsional mirror is actuated by a thin film coil.

10. The structure of claim **1** wherein a thin film coil is attached to said first side of said torsional mirror.

11. A method for making an integrated laser beam scanner comprising the steps of:

providing a wafer having a recess on a side;

attaching a layer having a first region and a second region to said side of said wafer having said recess;

fashioning a deflecting mirror from said first region of said layer;

fashioning a torsional mirror from said second region of said layer, said torsional mirror having a first side; and

mounting a semiconductor light emitter in said recess such that a light beam emitted from said semiconductor light emitter is deflected by said deflecting mirror onto said first side of said torsional mirror.

12. The method of claim **11** wherein said wafer is a silicon on oxide wafer.

13. The method of claim **11** wherein said layer is a single crystalline silicon layer.

14. The method of claim **11** wherein said semiconductor light emitter is mounted in said recess using solder bumps.

15. The method of claim **11** wherein said semiconductor light emftter is a VCSEL chip.

16. The method of claim **11** wherein said recess is deep reactive ion etched.

17. The method of claim **11** wherein said torsional mirror is actuated by a pair of electrodes.

18. The method of claim **11** wherein said torsional mirror is actuated by a thin film coil and an external magnetic field.

19. The method of claim **11** wherein a ferromagnetic thin film is attached to said first side of said torsional mirror.

20. The method of claim **11** wherein a thin film coil is attached to said first side of said torsional mirror.

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